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 1. **Beating in-order stalls with "flea-flicker" two-pass pipelining**

Barnes, R.D.; Sias, J.W.; Nystrom, E.M.; Patel, S.J.; Navarro, J.; Hwu, W.W.;
Computers, IEEE Transactions on
 Volume 55, Issue 1, Jan. 2006 Page(s):18 - 33
 Digital Object Identifier 10.1109/TC.2006.4

[AbstractPlus](#) | [Full Text: PDF\(1376 KB\)](#) IEEE JNL
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 2. **An analysis of the performance impact of wrong-path memory references on out-of-order execution processors**

Mutlu, O.; Kim, H.; Armstrong, D.N.; Patt, Y.N.;
Computers, IEEE Transactions on
 Volume 54, Issue 12, Dec. 2005 Page(s):1556 - 1571
 Digital Object Identifier 10.1109/TC.2005.190

[AbstractPlus](#) | [Full Text: PDF\(2120 KB\)](#) IEEE JNL
[Rights and Permissions](#)
 3. **Combined circuit and architectural level variable supply-voltage scaling for low power**

Hai Li; Chen-Yong Chér; Roy, K.; Vijaykumar, T.N.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
 Volume 13, Issue 5, May 2005 Page(s):564 - 576
 Digital Object Identifier 10.1109/TVLSI.2005.844295

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(688 KB\)](#) IEEE JNL
[Rights and Permissions](#)
 4. **Exploring the Performance Limits of Simultaneous Multithreading for Scientific Codes**

Athanasaki, E.; Anastopoulos, N.; Kourtis, K.; Koziris, N.;
Parallel Processing, 2006. ICPP 2006. International Conference on
 Aug. 2006 Page(s):45 - 54
 Digital Object Identifier 10.1109/ICPP.2006.41

[AbstractPlus](#) | [Full Text: PDF\(236 KB\)](#) IEEE CNF
[Rights and Permissions](#)
 5. **Quantifying and reducing the effects of wrong-path memory references in cache-coherent nr systems**

Sendag, R.; Yilmazer, A.; Yi, J.J.; Uht, A.K.;
Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International
 25-29 April 2006 Page(s):10 pp.

Digital Object Identifier 10.1109/IDPDS.2006.1639260

[AbstractPlus](#) | Full Text: [PDF\(216 KB\)](#) IEEE CNF

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6. **Workload characterization of biometric applications on Pentium 4 microarchitecture**

Chang-Bum Cho; Chande, A.V.; Yue Li; Tao Li;

[Workload Characterization Symposium, 2005. Proceedings of the IEEE International](#)
6-8 Oct. 2005 Page(s):76 - 86

Digital Object Identifier 10.1109/IISWC.2005.1526003

[AbstractPlus](#) | Full Text: [PDF\(468 KB\)](#) IEEE CNF

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7. **Techniques for efficient processing in runahead execution engines**

Onur Mutlu; Hyesoon Kim; Patt, Y.N.;

[Computer Architecture, 2005. ISCA '05. Proceedings. 32nd International Symposium on](#)
4-8 June 2005 Page(s):370 - 381

Digital Object Identifier 10.1109/ISCA.2005.49

[AbstractPlus](#) | Full Text: [PDF\(256 KB\)](#) IEEE CNF

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8. **Microarchitecture optimizations for exploiting memory-level parallelism**

Yuan Chou; Fahs, B.; Abraham, S.;

[Computer Architecture, 2004. Proceedings. 31st Annual International Symposium on](#)
19-23 June 2004 Page(s):76 - 87

Digital Object Identifier 10.1109/ISCA.2004.1310765

[AbstractPlus](#) | Full Text: [PDF\(389 KB\)](#) IEEE CNF

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9. **Using virtual load/store queues (VLSQs) to reduce the negative effects of reordered memory**

Jaleel, J.; Jacob, B.;

[High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on](#)
12-16 Feb. 2005 Page(s):191 - 200

Digital Object Identifier 10.1109/HPCA.2005.42

[AbstractPlus](#) | Full Text: [PDF\(200 KB\)](#) IEEE CNF

[Rights and Permissions](#)

10. **Checkpointed early load retirement**

Kirman, N.; Kirman, M.; Chaudhuri, M.; Martinez, J.F.;

[High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on](#)
12-16 Feb. 2005 Page(s):16 - 27

Digital Object Identifier 10.1109/HPCA.2005.9

[AbstractPlus](#) | Full Text: [PDF\(168 KB\)](#) IEEE CNF

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11. **Beating in-order stalls with "flea-flicker" two-pass pipelining**

Barnes, R.D.; Patel, S.J.; Nystrom, E.M.; Navarro, N.; Sias, J.W.; Hwu, W.W.;

[Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on](#)
2003 Page(s):387 - 398

Digital Object Identifier 10.1109/MICRO.2003.1253243

[AbstractPlus](#) | Full Text: [PDF\(373 KB\)](#) IEEE CNF

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12. **Reducing 3D wavelet transform execution time through the Streaming SIMD Extensions**

Bernabe, G.; Garcia, J.M.; Gonzalez, J.;

[Parallel, Distributed, and Network-Based Processing, 2003. Proceedings. Eleventh Euromicro Conf.](#)
5-7 Feb. 2003 Page(s):49 - 56

Digital Object Identifier 10.1109/EMPDP.2003.1183565

[AbstractPlus](#) | Full Text: [PDF\(338 KB\)](#) IEEE CNF

Rights and Permissions

13. Runahead execution: an alternative to very large instruction windows for out-of-order processing
Mutlu, O.; Stark, J.; Wilkerson, C.; Patt, Y.N.;
High-Performance Computer Architecture, 2003. HPCA-9. 2003. Proceedings. The Ninth International Conference on
8-12 Feb. 2003 Page(s):129 - 140
Digital Object Identifier 10.1109/HPCA.2003.1183532
[AbstractPlus](#) | Full Text: [PDF\(297 KB\)](#) IEEE CNF
[Rights and Permissions](#)
14. A superscalar RISC processor with 160 FPRs for large scale scientific processing
Shimada, K.; Kawashimo, T.; Hanawa, M.; Yamagata, R.; Kamada, E.;
Computer Design, 1999. (ICCD '99) International Conference on
10-13 Oct. 1999 Page(s):279 - 280
Digital Object Identifier 10.1109/ICCD.1999.808438
[AbstractPlus](#) | Full Text: [PDF\(28 KB\)](#) IEEE CNF
[Rights and Permissions](#)
15. Cooperative prefetching: compiler and hardware support for effective instruction prefetching in processors
Chi-Keung Luk; Mowry, T.C.;
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposium on
30 Nov.-2 Dec. 1998 Page(s):182 - 193
Digital Object Identifier 10.1109/MICRO.1998.742780
[AbstractPlus](#) | Full Text: [PDF\(180 KB\)](#) IEEE CNF
[Rights and Permissions](#)
16. A comparison of data prefetching on an access decoupled and superscalar machine
Jones, G.P.; Topham, N.P.;
Microarchitecture, 1997. Proceedings. Thirtieth Annual IEEE/ACM International Symposium on
1-3 Dec. 1997 Page(s):65 - 70
Digital Object Identifier 10.1109/MICRO.1997.645798
[AbstractPlus](#) | Full Text: [PDF\(508 KB\)](#) IEEE CNF
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